WHAT IS CLAIMED IS:

1. A gated MOS device which is resistant to failure in both high radiation environments and in SEE environments; said gated MOS device comprising a silicon die having a plurality of spaced trenches therein; each of said spaced trenches being defined by at least partly vertical walls joined at their bottoms by respective trench bases; at least portions of the areas of said vertical walls having a MOS gate dielectric thereon, said bases of said trenches having a bottom dielectric thereon; said gate dielectric having a thickness chosen to optimize resistance to high radiation effects; said bottom dielectric having a thickness greater than that of said gate dielectric and a thickness which is optimal for SEE resistance.

2. The gated MOS device of claim 1 in which said plurality of trenches are filled with conductive polysilicon which acts as a gate electrode.

3. The gated MOS device of claim 1 in which said gate dielectric and said bottom dielectric are both silicon dioxide.

4. The gated MOS device of claim 3 wherein said gate dielectric has a thickness which is less than 900 Å.

5. The gated MOS device of claim 3 wherein the thickness of said bottom dielectric is greater than about 1300 Å.

6. The gated MOS device of claim 4 wherein said gate dielectric thickness is about 500 Å.

7. The gated MOS device of claim 5 wherein said gate dielectric thickness is about 500 Å.

8. The gated MOS device of claim 5 wherein the thickness of said bottom dielectric is about 3000 Å.

9. The gated MOS device of claim 6 wherein the thickness of said bottom dielectric is about 3000 Å.

10. A trench MOS gated device which has improved resistance to both high radiation and SEE comprising a silicon wafer of one of the conductive types having a plurality of spaced shallow active trenches containing respective gate structures and a plurality of intermediate trenches each disposed between a respective pair of active trenches; each of said trenches having at least partly vertical walls joined at their bottoms by trench bottoms; each of said trenches containing a gate structure having a gate dielectric on at least portions of their said vertical walls, a bottom dielectric on their bottoms and a conductive polysilicon plug which acts as a gate electrode which contacts at least the interior surface of said gate dielectric; each of said

intermediate trenches having a shallow diffusion of the opposite conductivity extending from their walls and bottoms and being filled with a conductive polysilicon; the spaces between each of said trenches containing a channel region of the opposite conductivity and an upper source diffusion in contact with said polysilicon plugs in said trenches containing said gate structure; and a common source contact contacting each of said source regions and each of said conductive plugs in each of said intermediate trenches; a common gate electrode connected to each of said conductive plugs in each of said trenches containing a gate structure and a drain contact connected to the drift region beneath said trenches.

11. The device of claim 10 in which said polysilicon plugs in said trenches containing a gate structure is of said one of said conductivity types, and in which said polysilicon plugs in said intermediate trenches is of the opposite conductivity type.

12. The device of claim 10 wherein all of said trenches are parallel elongated trenches.

13. The device of claim 10 wherein at least a plurality of said trenches containing a MOS gated structure are polygonal in topology and are symmetrically spaced and disposed over the surface of said silicon wafer; said source regions surrounding respective ones of said trenches containing a MOS gated structure; said intermediate trenches consisting of a trench of lattice

shape in topology which extends in the space defined between spaced polygonal trenches.

14. The device of claim 12 in which said polysilicon plugs in said trenches containing a gate structure is of said one of said conductivity types, and in which said polysilicon plugs in said intermediate trenches is of the opposite conductivity type.

15. The device of claim 13 in which said polysilicon plugs in said trenches containing a gate structure is of said one of said conductivity types, and in which said polysilicon plugs in said intermediate trenches is of the opposite conductivity type.

16. The device of claim 10 wherein the thickness of said gate dielectric is chosen to optimize resistance to high radiation effects and wherein the thickness of said bottom dielectric is chosen to optimize resistance to SEE.

17. The device of claim 11 wherein the thickness of said gate dielectric is chosen to optimize resistance to high radiation effects and wherein the thickness of said bottom dielectric is chosen to optimize resistance to SEE.

18. The gated MOS device of claim 16 in which said gate dielectric and said bottom dielectric are silicon dioxide.

19. The gated MOS device of claim 18 wherein said gate dielectric has a thickness which is less than 900 Å.

20. The gated MOS device of claim 18 wherein the thickness of said bottom dielectric is greater than about 1300 Å.

21. The gated MOS device of claim 19 wherein the thickness of said bottom dielectric is greater than about 1300 Å.

22. A termination structure for a gated MOS device having an active area; said active area consisting of a plurality of spaced trenches in a common silicon die of one of the conductivity types, each of said trenches containing a respective MOS gate structure; the exterior trenches in said active area having a relatively high electric field at their bottom outer corners; said termination structure comprising a plurality of concentric ring-shaped trenches surrounding said active area and being spaced between said active area and the peripheral edge of said die; each of said plurality of ring-shaped trenches having a diffusion extending from their walls and bottom which is of the opposite conductivity type; each of said plurality of ring-shaped trenches having a conductive polysilicon plug of a conductivity of the opposite conductivity type; said active area having a common source contact; said

plurality of ring-shaped trenches being insulated from said source contact and comprising floating rings.

23. The termination structure of claim 22 wherein said concentric rings have a predetermined spacing from one another.

24. The termination structure of claim 23 wherein the spacing between said rings is selected to cause breakdown due to high reverse voltage to occur between said rings before it occurs in said active area.

25. The device of claim 10 which further contains a termination structure; said plurality of trenches containing a gate structure and said plurality of intermediate trenches defining an active area; said termination structure comprising a plurality of concentric ring-shaped trenches surrounding said active area and extending radially from said active area toward the edge of said die; each of said plurality of ring-shaped trenches having a diffusion extending from their walls and bottom which is of the opposite conductivity type; each of said plurality of ring-shaped trenches having a conductive polysilicon plug of a conductivity of the opposite conductivity type; said plurality of ring-shaped trenches being insulated from said source contact and comprising floating rings.

26. The termination structure of claim 25 wherein said concentric rings have a predetermined spacing from one another.

27. The termination structure of claim 26 wherein the spacing between said rings is selected to cause breakdown due to high reverse voltage to occur between said rings before it occurs in said active area.

28. The device of claim 16 which further contains a termination structure; said plurality of trenches containing a gate structure and said plurality of intermediate trenches defining an active area; said termination structure comprising a plurality of concentric ring-shaped trenches surrounding said active area and extending radially from said active area toward the edge of said die; each of said plurality of ring-shaped trenches having a diffusion extending from their walls and bottom which is of the opposite conductivity type; each of said plurality of ring-shaped trenches having a conductive polysilicon plug of a conductivity of the opposite conductivity type; said plurality of ring-shaped trenches being insulated from said source contact and comprising floating rings.